(2 pts) Name:

AME 3623: Embedded Real-Time Systems

Midterm Exam

Solution Set

March 29, 2005

Problem	Topic	Max	Grade
0	-	2	
1	Digital Logic	37	
2	Arithmetic	36	
3	Finite State Machines	25	
Total			

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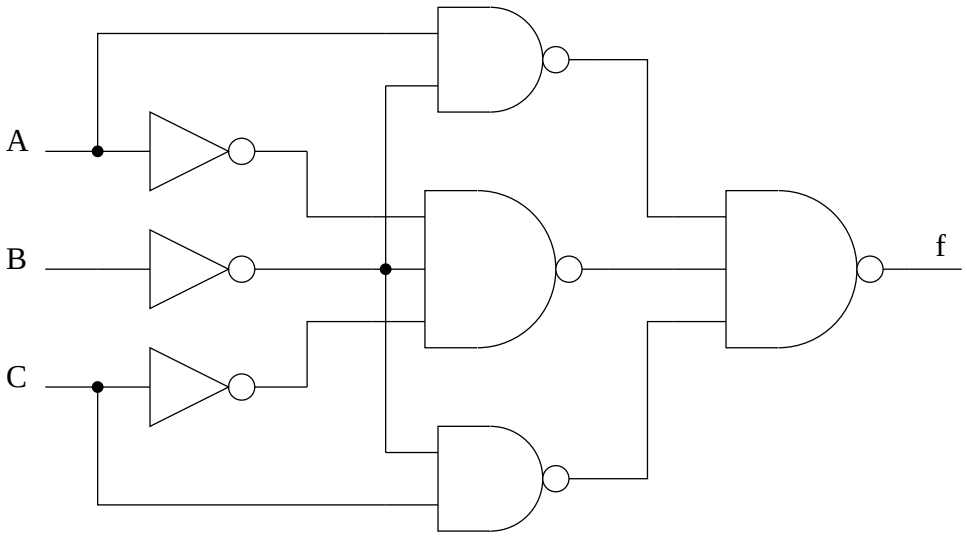
1. **Digital Logic** (37 pts)

Given the following circuit:



(a) (10 pts) Show the corresponding truth table.

A	B	C	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

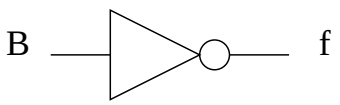
(b) (7 pts) Give the Karnaugh map and show the clusters.

C \ AB	00	01	11	10
0	1	0	0	1
1	1	0	0	1

(c) (5 pts) What is the minimum algebraic description for f?

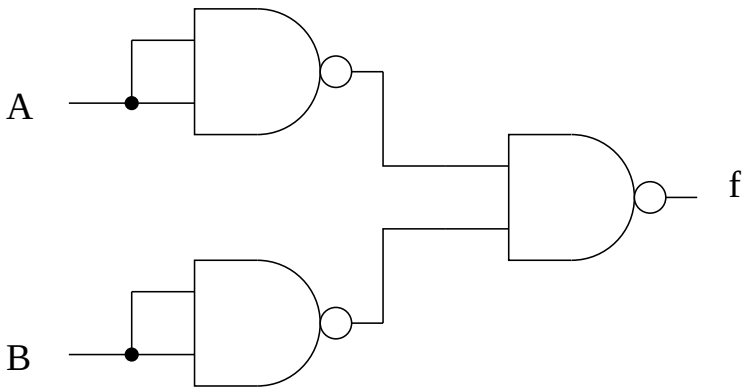
$f = \overline{B}$

(d) (5 pts) Draw the corresponding circuit.



(e) (10 pts) (separate question) Using only 2-input NAND gates, design a 2-input OR circuit.

By DeMorgen's Law: $A + B = \overline{\overline{A} * \overline{B}}$. *So: we need to invert* A *and* B*, and then use these as inputs to a NAND gate. We can also use NAND gates as inverters.*



2. **Arithmetic** (36 pts)

Given the following number in hexadecimal: $E5$. Assume that this is a two's complement, 8-bit number.

(a) (2 pts) What is the sign of this number?

$E5 = 11100101$

This is a negative number (the most significant bit is a 1*).*

(b) (5 pts) What is the decimal equivalent of this number?

The additive inverse of this number is: 00011011

The decimal equivalent of this is: $16 + 8 + 2 + 1 = 27$

So the decimal equivalent of the original number is -27

(separate question) Given two numbers (in decimal): $X = 11$ and $Y = 23$

(c) (9 pts) What are the binary equivalents of these numbers? Assume an 8-bit, twos complement representation.

$X = 00001011$

$Y = 00010111$

(d) (5 pts) What is the additive inverse of Y?

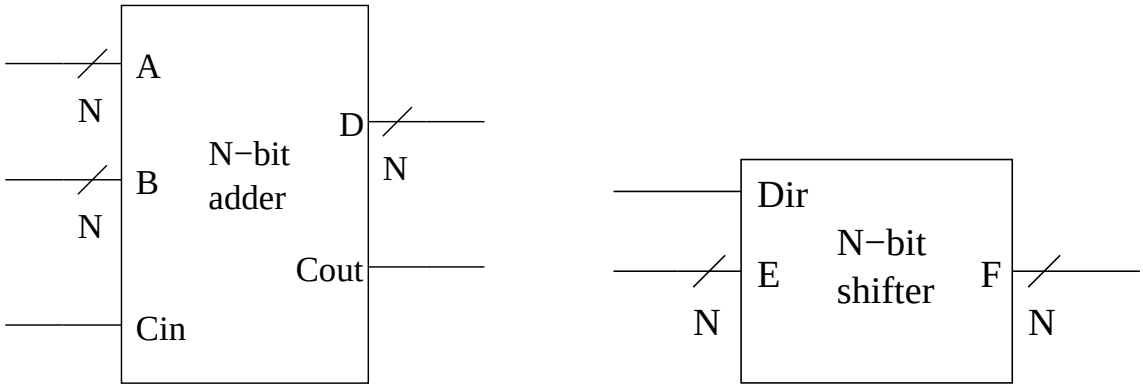
$-Y = 11101001$

(e) (5 pts) Subtract Y from X in binary (show your work)

We simply need to add X and $-Y$:

$$\begin{array}{r} 00001011 \\ +11101001 \\ \hline 11110100 \end{array}$$

(separate question) Given an N-bit adder device and an N-bit shifter device:

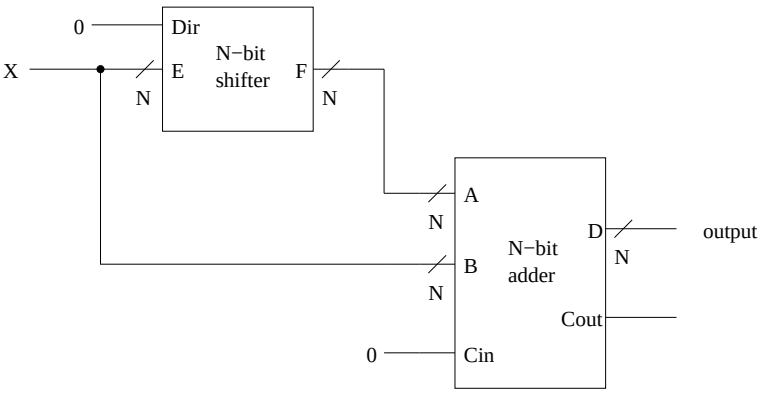


The N-bit adder takes three inputs A, B, and C_{in}, and produces two outputs D and C_{out}.

The N-bit shifter takes two inputs E and Dir, and produces an output F. When $Dir = 0$, the device shifts E to the right; when $Dir = 1$, the device shifts E to the left.

(f) (10 pts) Design a circuit that takes as input an N-bit number X and produces as output $X * 1.5$ (you may assume that you are working with unsigned binary).

There are a variety of solutions; here is one: add X to $X/2$. We can divide a number by two by shifting its binary represention to the right.



3. **Finite State Machines** (25 pts)

Assume a 3-bit binary device that can execute the following operations on the downward edge of the clock:

- Increment the number by 3, and
- Take the additive inverse (in twos complement) of the number.

Design a Finite State Machine representation of this device using the following steps:

(a) (5 pts) What are the states?

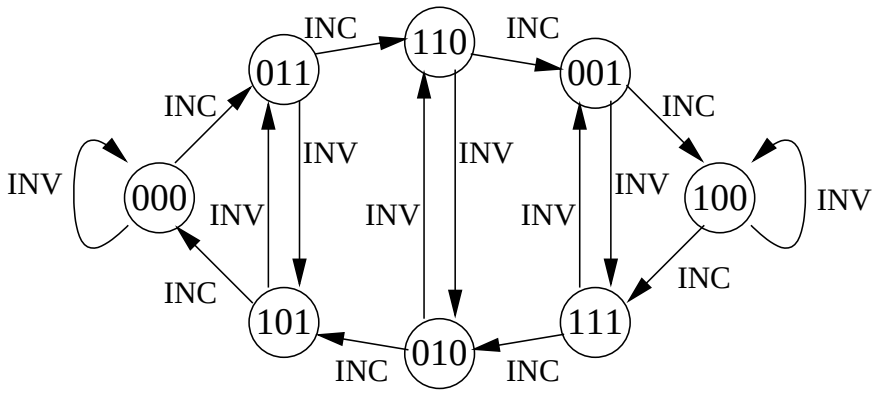
All combinations of the individual bit values (there are 8 in total):
$000, 001, 010, 011, ...111$

(b) (5 pts) What are the events?

Increment *(INC) and* **invert** *(INV). Note that these events arrive on the downward edge of the clock.*

(c) (5 pts) What are the outputs?

Same as the states.

(d) (10 pts) Show the full state transition diagram.

Since the outputs are the same as the states (specifically, the state being transitioned to), we will not include them in the diagram.