(2 pts) Name:

AME 3623: Embedded Real-Time Systems

Midterm Exam

Solution Set

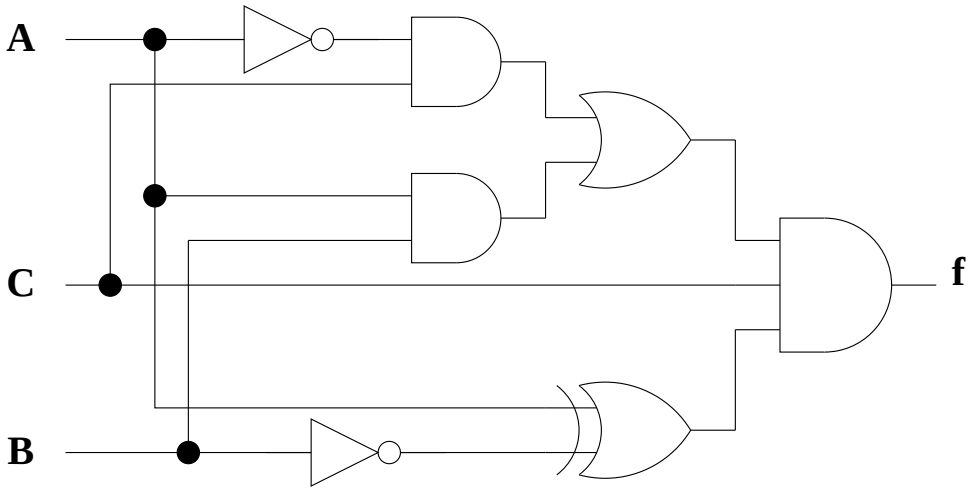
March 9, 2006

Problem	Topic	Max	Grade
0	-	2	
1	Digital Logic	37	
2	Number Systems	15	
3	Sequential Logic and Finite State Machines	20	
4	Memory	10	
5	Microcontroller I/O	18	
Total			

---

1. **Digital Logic** (37 pts)

Given the following circuit:



(a) (10 pts) Show the corresponding truth table.

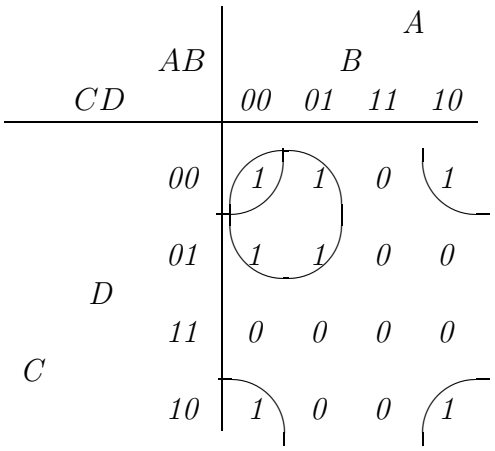
A	B	C	f
0	*0*	*0*	*0*
0	*0*	*1*	*1*
0	*1*	*0*	*0*
0	*1*	*1*	*0*
1	*0*	*0*	*0*
1	*0*	*1*	*0*
1	*1*	*0*	*0*
1	*1*	*1*	*1*

Observations: $C = 0$ *implies that* $f = 0$. $A \neq B$ *implies that* $f = 0$.

Given the following truth table:

A	B	C	D	f
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

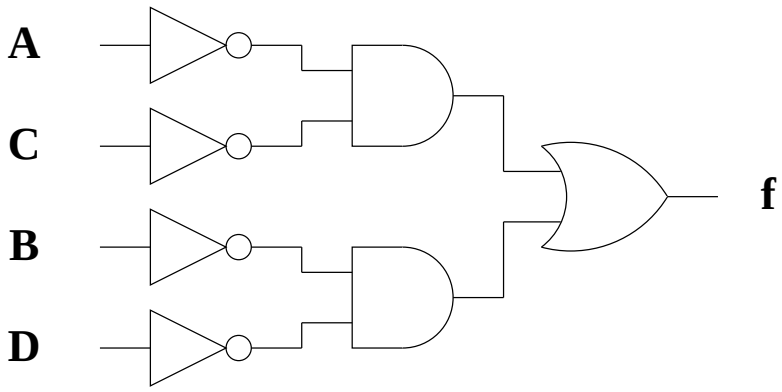
(b) (7 pts) Give the Karnaugh map and show the clusters.



(c) (5 pts) What is the corresponding algebraic description for f (that comes directly from the clusters)?

$f = \overline{A}\,\overline{C} + \overline{BD}$

(d) (5 pts) Draw the corresponding circuit.



(e) (10 pts) Prove that $A \oplus \overline{B} = \overline{A \oplus B}$

$$
\begin{aligned}
A \oplus \overline{B} &= A\overline{\overline{B}} + \overline{A}\,\overline{B} && \textit{XOR definition} \\
&= AB + \overline{A}\,\overline{B} && X = \overline{\overline{X}} \\
&= \overline{\overline{AB} * \overline{\overline{A}\,\overline{B}}} && \textit{DeMorgen's Law} \\
&= \overline{(\overline{A} + \overline{B}) * (\overline{\overline{A}} + \overline{\overline{B}})} && \textit{DeMorgen's Law} \\
&= \overline{(\overline{A} + \overline{B}) * (A + B)} && X = \overline{\overline{X}} \\
&= \overline{\overline{A}A + \overline{B}A + \overline{A}B + \overline{B}B} && \textit{Distributive Law} \\
&= \overline{\overline{B}A + \overline{A}B} && Y + \overline{X}X = Y \\
&= \overline{A \oplus B} && \textit{XOR definition}
\end{aligned}
$$

2. **Number Systems** (15 pts)

Given the following number in hexadecimal: $2E$.

(a) (5 pts) What is the binary equivalent of this number?

$0x2E = 101110$

(b) (5 pts) What is the decimal equivalent of this number?

The decimal equivalent of this is: $32 + 8 + 4 + 2 = 46$

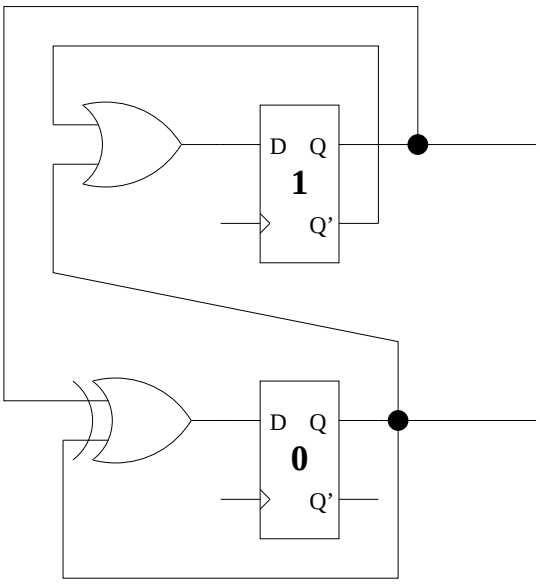
(separate question) Given the decimal number 178:

(c) (5 pts) What is the binary equivalent of this number? (show your work)

value	**binary**	i	2^i
178	*00000000*		
		7	*128*
50	*10000000*		
		5	*32*
18	*10100000*		
		4	*16*
2	*10110000*		
		1	*2*
0	*10110010*		

3. **Sequential Logic** (20 pts)

Given the following circuit:



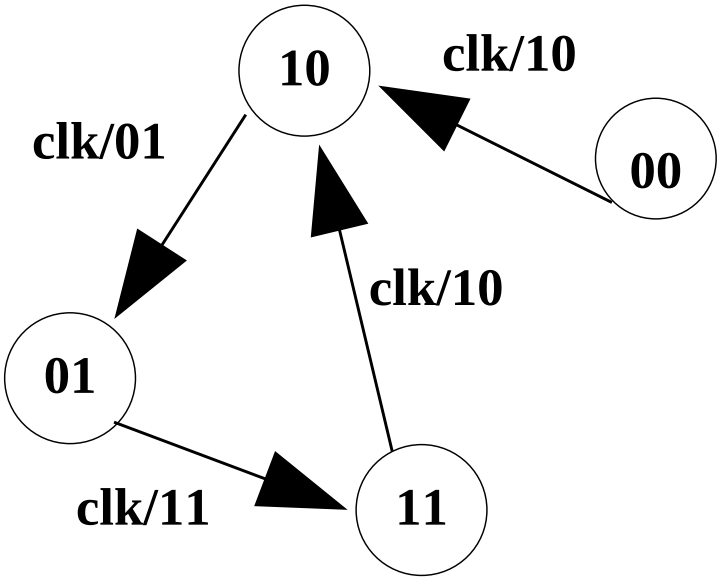
(a) (5 pts) What are the possible states (list all of them)?

All combinations of the individual bit values (there are 4 in total):
$00, 01, 10, 11$

(b) (10 pts) Assume an initial state of $Q1 = 0$ and $Q0 = 1$. What is the sequence of states over 5 clock cycles?

01, 11, 10, 01, 11, 10

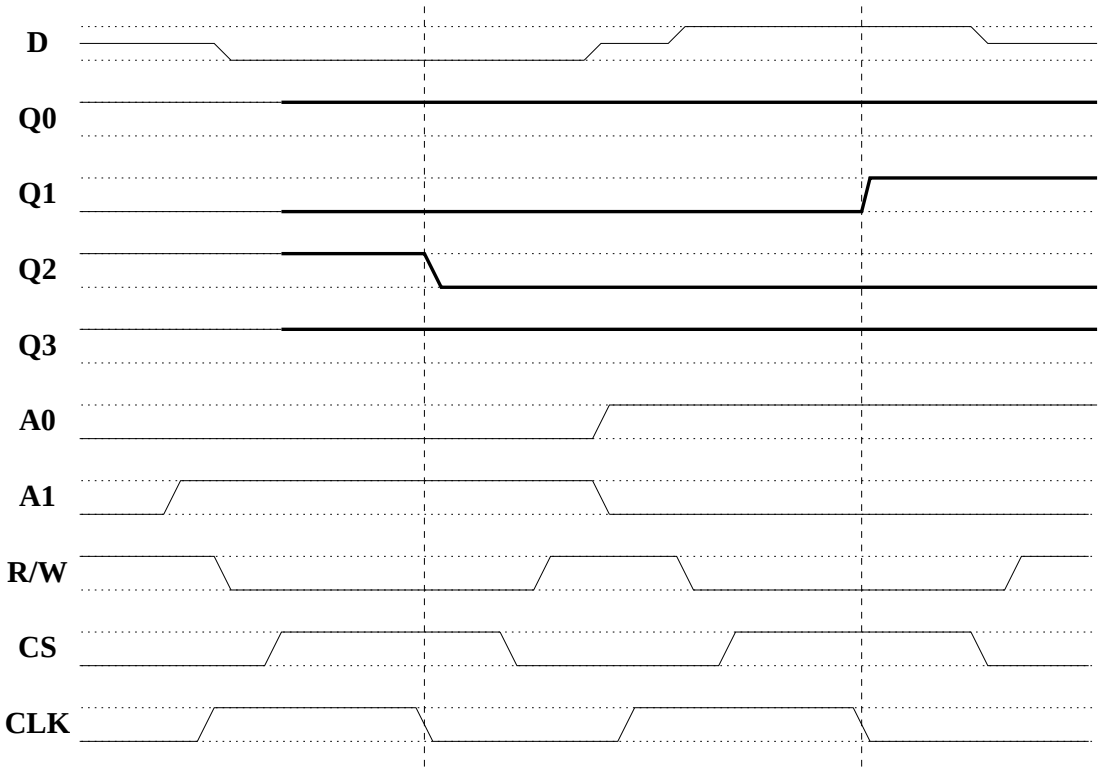
(c) (5 pts) Draw the finite state machine representation of this circuit.



(In this case, I will accept your answer if you did not place the output labels on the transitions).

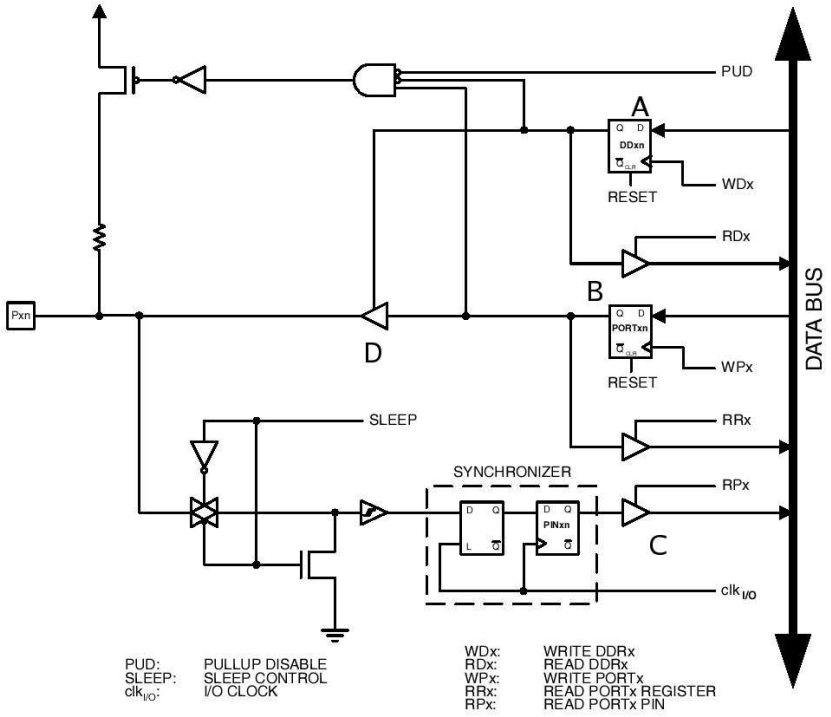
4. **Memory** (10 pts)

(a) (10 pts) For the timing diagram below, fill in the missing traces.



Both memory operations are write operations (to elements 3 and 0, respectively). Note, however, that the state of Q0 does not change (it was already in a state of "1").

5. **Microcontroller I/O** (18 pts)



(a) (8 pts) Identify component "C". Explain in brief the function of this type of component (in general, not in this circuit).

Component C is a tristate buffer. When the select line (labeled "RPx" in the figure) is high, the buffer drives the output with the value from the input. When the select line is low, the buffer does not affect the state of the output line. (this select behavior allows us to connect the outputs of several buffers together – as in a bus)

(b) (10 pts) What effect does the following code have on the state of this circuit (in terms of components A, B, C, and D)? State any assumptions that you must make.

```
PORTB = PORTB | 0x10;
```

This code sets bit 4 (counting from 0) of PORTB (component B) to 1. If flip-flop A is in a state of 1, then the output of component D will now be 1 (otherwise, it is left in a floating state). Components A and C do not change state.