AME 3623: Embedded Real-Time Systems: Final Exam

May 9, 2006

- This examination booklet has 14 pages.
- Do not forget to write your name at the top of the page and to sign your name below.
- The exam is closed book, closed notes, and closed electronic device. The exception is that you may have one page of your own notes.
- The exam is worth a total of 200 points (and 20% of your final grade).
- Explain your answers clearly and be concise. Do not write long essays (even if there is a lot of open space on the page). A question worth 5 points is only worth an answer that is at most 1.5 sentences.
- You have 2 hours to complete the exam. Be a smart test taker: if you get stuck on one problem go on to the next. Don't waste your time giving details that the question does not request. Points will be taken off for answers containing extraneous information.
- Show your work. Partial credit is possible, but only if you show intermediate steps.

Topic	Max	Grade
-	2	
Interrupts and I/O	40	
Multi-Tasking	46	
Finite State Machines	45	
Analog Processing	28	
Microprocessor Design	15	
Logic	26	
	202	
	- Interrupts and I/O Multi-Tasking Finite State Machines Analog Processing Microprocessor Design	-2Interrupts and I/O40Multi-Tasking46Finite State Machines45Analog Processing28Microprocessor Design15Logic26

On my honor, I affirm that I have neither given nor received inappropriate aid in the completion of this exam.

Signature: _____

Date: _____

1. Interrupts and I/O

(a) (5 pts) Define (in brief) "bus arbitration."

(b) (10 pts) For the given clock rate and prescaler configuration of the mega8 timer0, give the time (in microseconds) between interrupts (reduced fractions and exponents of 2 are fine).

Prescaler	1 MHz clock	16 MHz clock
No prescaler		
Div 8		
Div 64		
Div 256		
Div 1024		

(c) (6 pts) List at least three operations that are performed by the processor in response to an interrupt

(d) (5 pts) Explain (in brief) the purpose of a buffer.

(e) (14 pts) Below is an interrupt routine that is supposed to produce a pulse-widthmodulated signal on port C, pin 5 (counting from 0). However, there exist several bugs (errors). Make the necessary changes to this code to remove these bugs. The frequency should be constant; the width of the pulse is specified by the variable **duration**. You may assume that the hardware has been initialized correctly.

```
volatile unit8_t counter;
volatile uint8_t duration; // Duration of the high side of the pulse
SIGNAL(SIG_OVERFLOWO) {
   ++counter;
   if(counter == 0)
     PORTB &= 0x10; // Turn on line
   if(counter <= duration) {
     PORTB |= ~0x10; // Turn line off
     counter = 0;
   }
}
```

2. Multi-Tasking

(a) (8 pts) List two necessary conditions for there to be a shared data problem.

(b) (8 pts) What is the distinction between a process and a processor?

Consider three processes that are involved in the control of a helicopter:

- **Planner** uses information about the current location of the craft, the surrounding terrain, and the immediate goals to determine a course of flight. This computation is performed once per second and requires 400ms to execute.
- Yaw Control takes input from a digital compass at 20Hz, filters this signal, and computes a rudder command. This computation requires 10ms in the worst case.
- Local Navigation takes input from a camera, processes the images, and produces lateral velocity signals. This process needs to be scheduled at 5Hz and requires 50ms in the worst case.
- (c) (15 pts) Show the schedule that results from a round-robin, timesliced scheduler for time 0 through time 160ms (show both "running" and "ready" processes). Assume timeslice duration of 10ms, and that the processes are initially in the ready queue as ordered above. Also assume that at the end of a timeslice, the exiting process (if it still needs to execute) is placed on the ready queue before any newly-scheduled processes.

(d) (15 pts) Show the schedule (including "running" and "ready" processes) that results from the Rate Monotonic Scheduling algorithm.

3. Finite State Machines

Consider a robot that is facing down a hallway and has the ability to detect doorways using a sensor that is mounted on a turret (not unlike the turrets on our robots). In addition, the robot is able to detect when it runs into a wall. Assuming an ability to make perfect movements, we will design a finite state machine that will take the robot to the third door on the left side of the hallway, turn, enter it, and stop (the robot knows that it has moved through the door when it can no longer "see" the door in front of it). In addition, if there is ever a collision, the robot should stop and signal an error condition.

(a) (5 pts) What are the states?

(b) (5 pts) What are the events?

(c) (5 pts) What are the actions? You are responsible for motion of the robot and of the turret (you may separate these in your action list).

(d) (10 pts) Show the finite state machine.

Suppose that instead of the third door from the robot's initial location, we want to move to the third door from the end of the hallway (along the same direction as the robot's initial orientation). Modify your FSM design to accommodate this.

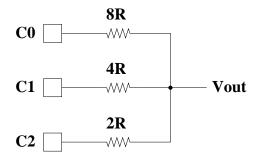
(e) (5 pts) What are the additional states?

(f) (5 pts) What are the additional actions?

(g) (10 pts) Show the modified FSM.

4. Analog Processing

Consider the following digital-to-analog conversion circuit:



(a) (10 pts) Give the expression for V_{out} in terms of binary digits C0, C1, and C2.

(b) (8 pts) Given that a process wants to generate a voltage $V_{out} = 4V$. What choice of binary values could it use to best approximate this value?

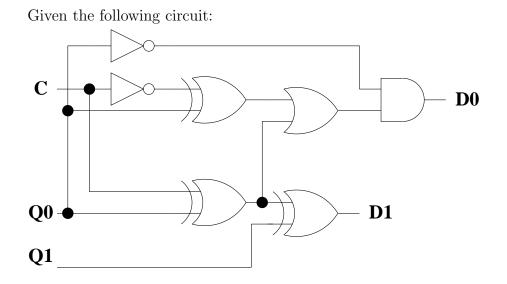
(c) (10 pts) Assume an analog-to-digital converter that uses successive approximation to estimate the digital equivalent of an input voltage. Assume also that the 3-bit digital-to-analog converter from above is used. Given an input voltage of 2V, show the steps taken by the successive approximation algorithm, as well as its final choice.

5. Microprocessor Design

(a) (5 pts) What is the function of the program counter?

(b) (5 pts) What is the function of the general-purpose registers?

(c) (5 pts) (True/False) The clock signal is used by a RAM during a "read" operation from the device. Explain.

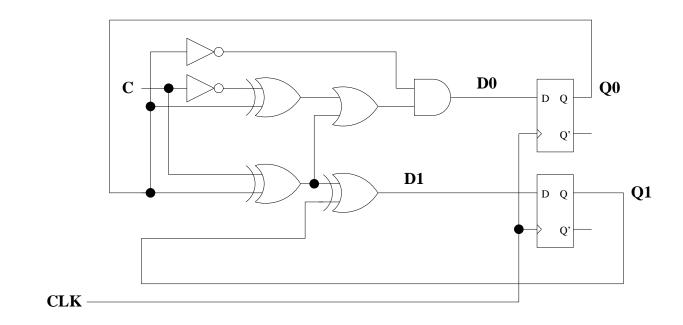


(a) (10 pts) What is the truth table?

C	Q1	Q0	D1	D0
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

(b) (8 pts) Give the simplified algebraic expression for D0

Now consider the following circuit:



(c) (8 pts) Assume that C = 1 and the initial state is Q1 = 1 and Q0 = 0. What is the sequence of states for five clock ticks (*CLK* transitions from high to low)?